## **REMARKS**

Claims 1-10 are pending in the current application. In the Office Action dated August 22, 2006, the Examiner objected to claim 6, rejected claim 4 under 35 U.S.C. § 112, second paragraph, rejected claims 1, 2, 4, 6, 8, 9, and 10 under 35 U.S.C. § 102(b) as being clearly anticipated by Uming U-Ming Ko, European Patent Application 0 419 105 A2 ("Ko"), and rejected claims 3 and 7 under 35 U.S.C. § 103(a) as being unpatentable over Ko in view of Alexander, U.S. Patent No. 5,953,684 ("Alexander"). Applicants' representative has amended the claims to address the Examiner's objections and 35 U.S.C. § 112, second paragraph, rejection. Applicants' representative respectfully traverses the 35 U.S.C. § 102(b) and 35 U.S.C. § 103(a) rejections.

Claim 1 is provided, below, for the Examiner's convenience:

- 1. A subsystem controller implemented as a single integrated circuit for control of a device or subsystem within an electronic system having system processing components, the subsystem controller comprising:
- a complex programmable logic device that can be programmed to provide logic circuits that implement control functionality;
- a micro-controller that can execute software routines that implement control functionality;
- read-only memory that stores executable code for execution by the micro-controller;
- random-access memory that can store data and executable code for execution by the micro-controller;
- a bus interface for exchanging data and control signals between the subsystem controller and system processing components; and
- an additional electronic interface to a device or subsystem controlled by the subsystem controller. (emphasis added)

On page 1 of the current application, the phrase "subsystem controller" is clearly defined as follows:

The term "subsystem controller" generally refers to a subcomponent of a more complex electronic system, such as a computer, that comprises logic circuits, a programmable logic device, and a general-purpose micro-controller that executes a number of software routines. A subsystem controller is generally dedicated to one or a small number of specific control tasks. For example, the control of LED and LCD display devices incorporated in a front panel display of a computer system is generally carried out by one or more subsystem controllers. Use of subsystem controllers may offload computationally intensive and time-intensive tasks from the main processor or processors of computer systems, and may

significantly decrease data traffic on critical busses of the computer system that are bottlenecks for data movement within the computer system.

Claim 1 recites a "subsystem controller implemented as a single integrated circuit for control of a device or subsystem within an electronic system having system processing components" that includes "a complex programmable logic device that can be programmed to provide logic circuits that implement control functionality" and "a microcontroller that can execute software routines that implement control functionality."

The Examiner reads the claim 1 element "a micro-controller that can execute software routines that implement control functionality" onto the following language, on line 55 of column 1 to line 6 of column 2, of Ko's Summary of the Invention: "remainder of the semiconductor substrate" that "is available for additional peripheral circuitry to implement necessary circuitry to allow the digital signal processor to perform complex microcontroller and other applications without the degradation in speed associated with systems requiring interchip communications." The Examiner also reads the claim 1 element "a micro-controller that can execute software routines that implement control functionality" onto element 1 of Figure 12, described by Ko, on lines 49-50 of column 2, as a digital signal processor. The first part of the Summary of the Invention describes the present inventions as "a monolithic integrated circuit" which "contains an embedded digital signal processor." Thus, the "remainder of the semiconductor substrate" in the language onto which the Examiner reads the claim 1 element "a micro-controller that can execute software routines that implement control functionality" is the non-digital-signal-processor portion of the monolithic integrated circuit disclosed by Ko. In other words, the Examiner reads the claim 1 element "a micro-controller that can execute software routines that implement control functionality" onto both Ko's embedded digital signal processor as well as onto the portion of Ko's monolithic integrated circuit that is not the digital signal processor. This rejection makes no sense. For this reason, alone, the 35 U.S.C. § 102(b) fails.

In fact, Ko's monolithic integrated circuit does not anticipate, and is unrelated to, the Applicants' claimed subsystem controller. A quick perusal of Wikipedia definitions obtained from the Wikipedia web site provides the following definitions:

A digital signal processor (DSP) is a <u>specialized microprocessor</u> designed specifically for <u>digital signal processing</u>, generally in <u>real-time</u>.

**Digital signal processing (DSP)** is the study of <u>signals</u> in a <u>digital</u> representation and the processing methods of these signals. DSP and <u>analog signal processing</u> are subsets of <u>signal processing</u>. It has three major subfields: <u>audio signal processing</u>, <u>digital image processing</u> and <u>speech processing</u>.

The main article for this <u>category</u> is <u>Digital signal processing</u>.

## **Subcategories**

There are 5 subcategories to this category shown below (more may be shown on subsequent pages).

A

• [+] <u>Audio editors</u>

F

• [+] FFT algorithms

I

• [+] Image processing

S

• [+] Speech recognition

 $\mathbf{W}$ 

• [+] Wavelets

As is well-known, in the electronic arts, a digital signal processor is a specialized microprocessor that is used to execute mathematical operations related to signal processing, including the audio-editing-related, FFT-related, image-processing-related, speech-recognition-related, and wavelet-related operations discussed above. A digital signal processor is not a subsystem controller, and is not capable of executing software routines that implement control functionality. Thus, Ko's embedded digital signal processor is entirely unrelated to the currently claimed subject matter. Ko has combined

a digital signal processor with "additional peripheral circuitry." Ko's monolithic integrated circuit is a digital signal processor with additional functionality.

By contrast, as clearly described in the current application, Applicants' claimed subsystem controller is, in fact, a subsystem controller, implemented on both "a complex programmable logic device that can be programmed to provide logic circuits that implement control functionality" and "a micro-controller that can execute software routines that implement control functionality." Both the programmable logic and the microprocessor are used to implement subsystem controller functionality. As clearly discussed in the current application beginning on line 20 of page 6, and as illustrated in Figure 2 of the current application, Applicants' subsystem controller partitions subsystem-controller processing between programmable logic and a microprocessor.

Ko does not partition subsystem controller functionality, or any other functionality, between the digital signal processor and the additional peripheral circuitry. Ko describes possibilities for the additional peripheral circuitry, beginning on line 5 of column 4, that include ROM, RAM, and circuits that interface the digital signal processor with other components. Ko does not teach, mention, or suggest that the additional peripheral circuitry would be used to implement a digital signal processor. It would exceedingly strange to do so, since digital signal processors are designed to extremely efficiently and rapidly carry out signal-processing activities - far faster than any gatearray could be configured to execute similar signal-processing activities. Thus, Ko does not, and cannot, teach or suggest partitioning digital signal processing between Ko's digital signal processor and Ko's additional peripheral circuitry. According to the above definitions, and as well known to those familiar with electronics and computing, a digital signal processor is a specialized microprocessor that carries out signal-processing operations, and cannot be used as a subsystem controller. Therefore, Ko does not teach or suggest partitioning any kind of controller functionality between the digital signal processor and the additional peripheral circuitry.

In additional claim rejections, the Examiner suggests that Ko's digital signal processor can execute controller software routines. It cannot, as discussed above. In the rejection of claim 6, the Examiner reads the phrase "single-IC subsystem controller" onto Figure 1 of Ko. Figure 1 is a block diagram of a digital signal processor

embedded within a monolithic integrated circuit. It is, as discussed above, a digital signal processor. In the rejection of claim 6, the Examiner states that ROM 14 within Ko's digital signal processor read on the language "implementing software routines for execution by a micro-controller within the single-IC subsystem controller." ROMs do not implement software. The ROM referred to by the Examiner is a read-only memory that stores digital-signal-processing routines executed by the digital signal processor. Because independent claims 1 and 6 are not anticipated by, or even related to, Ko, none of dependent claims 2-6 and 7-10 are anticipated by, or related to, Ko.

In summary, Ko discloses a digital signal processor, while the current application is directed to a subsystem controller. Ko is unrelated to the subsystem controller to which the current claims are directed.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted, Michael B. Raynham et al. Olympic Patent Works PLLC

Robert W. Bergstrom

Registration No. 39,906

Enclosures: Postcards (2) Transmittal in duplicate

Olympic Patent Works PLLC P.O. Box 4277 Seattle, WA 98194-0277 206.621.1933 telephone 206.621.5302 fax